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Mixed-mode simulation is handled on three levels; (a) with primitive digital elements that use timing models and the built-in 12 or 16 state digital logic simulator

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mixed-mode simulator; two-tier hierarchical approach; IEEE TERMS. Circuit optimization; Circuit simulation; Very large scale integration

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Simulation Tools for VLSI Logic and Mixed-mode Simulation for A MOS Modelling Technique for 4-State True-Value Hierarchical Logic Simulation

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the simulator is capable of performing full mixed-level and mixed-mode hierarchical piecewise linear simulator T.A.M VLSI circuit simulator.

Uwvlsi - cadence_mixed_signal

Mixed Signal Simulations with Create a hierarchy view the simulator may have trouble running in digital mode. This would make the simulation very slow.

Panda-a hierarchical mixed mode vlsi module

PANDA-a hierarchical mixed mode VLSI module assembler 1989 Proceedings of the IEEE Custom Integrated Circuits Conference. Rocznik. 1989. Strony. 23.7/1

Patent us6577992 - transistor level circuit

the hierarchical simulation netlist is typically VLSI circuits designed "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power

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